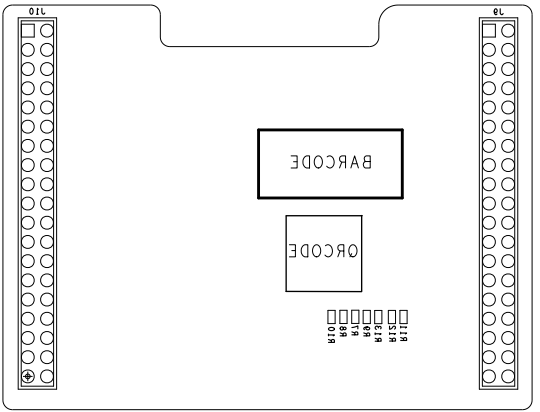
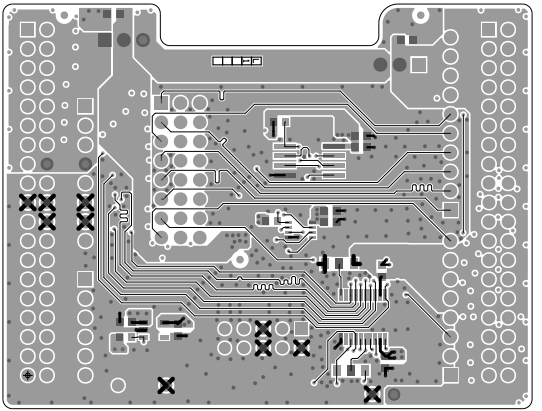


CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: ASSEMBLY BOTTOM		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

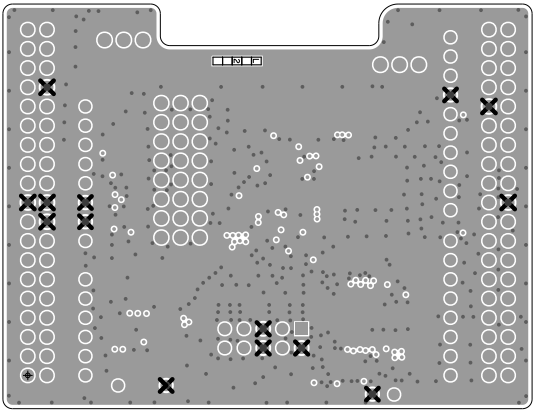
ART FILM - TOP



CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: TOP SIDE		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

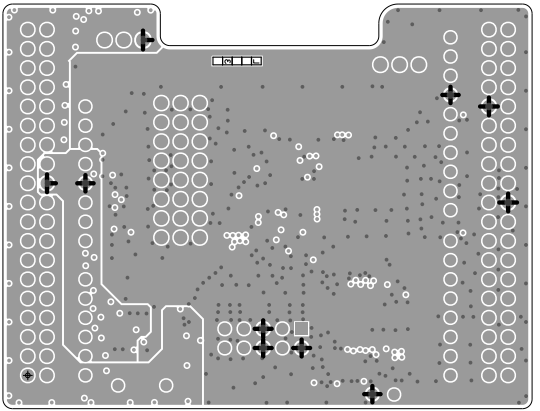
ART FILM - TOP

ART FILM - L2_GND

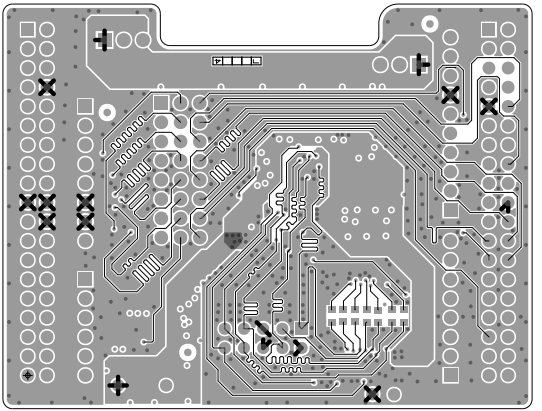


CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: L2_GND		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

ART FILM - L2_GND

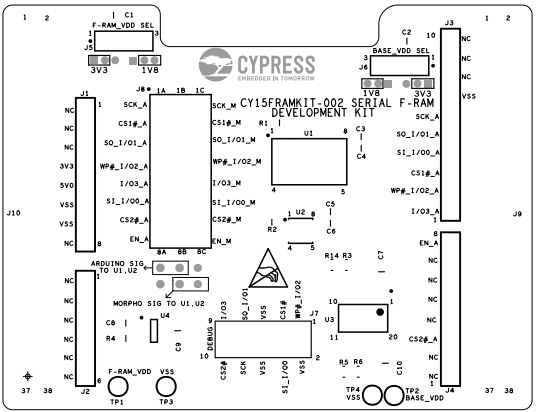


CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: L3_PWR		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19



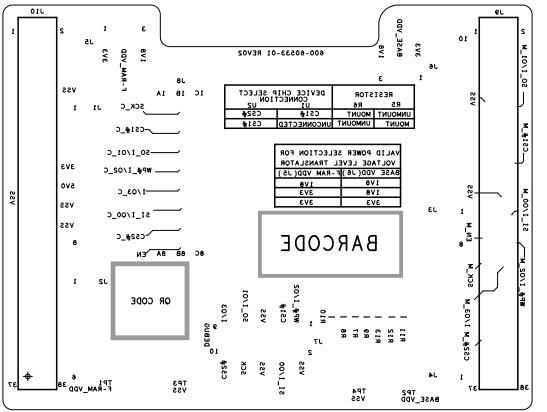
CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: BOTTOM SIDE		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

ART FILM - SST



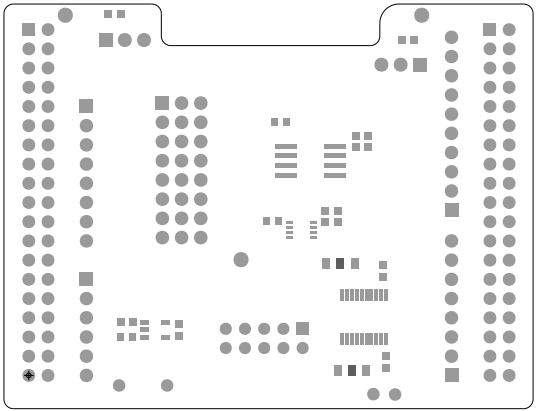
CYPRESS EMBEDDED IN TOMORROW	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: SILKSCREEN TOP		
SAN JOSE, CA 95134 (408) 943-2600	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

ART FILM - SST



CYPRESS EMBEDDED IN TOMORROW	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: SILKSCREEN BOTTOM		
SAN JOSE, CA 95134 (408) 943-2600	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

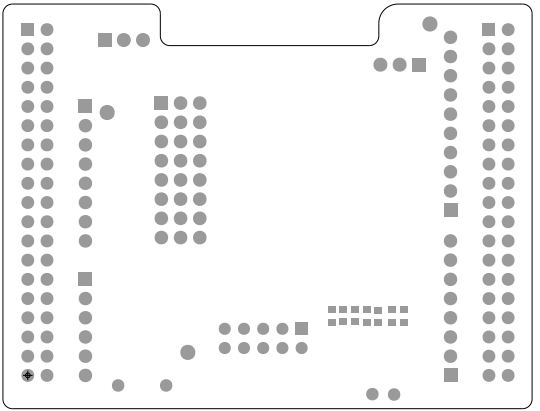
ART FILM - SMT



CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: SOLDERMASK TOP		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

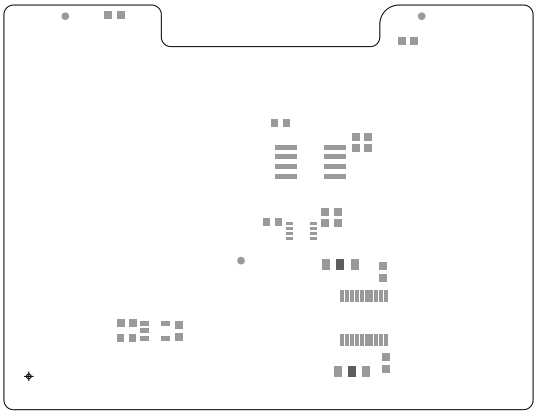
ART FILM - SMT

ART FILM - SMB



CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: SOLDERMASK BOTTOM		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

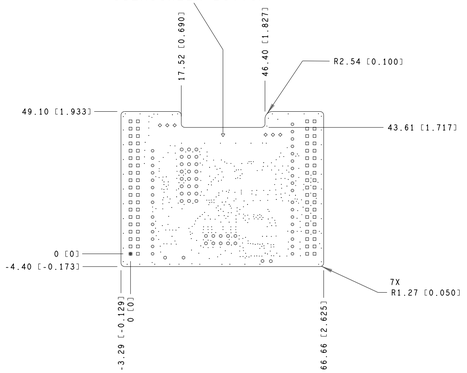
ART FILM - SMB



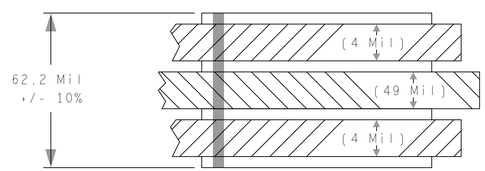
CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: SOLDERPASTE TOP		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

ART FILM - Detail1

DATE CODE & UL MARKING
SILKSCREEN BOTTOM



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
-	10.0	+3.0/-10.0	PLATED	460
□	39.37	+3.0/-3.0	PLATED	76
○	40.0	+3.0/-3.0	PLATED	32
○	43.0	+3.0/-3.0	PLATED	14
○	43.31	+3.0/-3.0	PLATED	24
○	63.78	+3.0/-3.0	PLATED	6



LAYER DESCRIPTION	START COPPER WT	SE IMP OHMS	SE TRACE WIDTH	REF LAYER	CPW SPACE	DIFF IMP OHMS	DIFF TRACE WIDTH/SPACE	REF LAYER	CPW SPACE
L01 - TOP	1.0 OZ	50	5 Mil	L2	-NA-	-NA-	-NA-	-NA-	-NA-
L02 - GND PLANE	1.0 OZ	-NA-	-NA-	-NA-	-NA-	-NA-	-NA-	-NA-	-NA-
L03 - PWR PLANE	1.0 OZ	-NA-	-NA-	-NA-	-NA-	-NA-	-NA-	-NA-	-NA-
L04 - BOTTOM	1.0 OZ	50	5 Mil	L3	-NA-	-NA-	-NA-	-NA-	-NA-

STACK-UP

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:
   A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES 610-60533-01_02.ZIP.
   B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
   C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES, INCLUDING NON-FUNCTIONAL PADS, IS NOT ALLOWED, AND THE DESIGN OF ALL PLANE STRUCTURES MUST BE MAINTAINED TO ENSURE PROPER ELECTRICAL PERFORMANCE.
   D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
   E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
   F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:
   A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS).
   B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF.076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
   C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
   D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK.

3. DRILLING:
   A. VIA DIAMETERS (TOL. = +.051/- DRILL DIAMETER [+.0020/- DRILL DIAMETER]) SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS SHALL BE VERIFIED AT FINAL INSPECTION.
   B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:
   A. APPLY LPI SOLDER MASK USING PROVIDED DATA.
   B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR BLUE.
   C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. MARKING:
   A. MARK PCB PER PROVIDED DATA USING SILKSCREEN OR AUTOMATED INJET PROCESSING WITH PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL BE APPLIED USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
   C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE.

6. ELECTRICAL TEST:
   A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING SUPPLIED VALOR ODB++ DATABASE, OR GERBER DATA AND AN IPC-D-356 NETLIST.
   B. ALL PCBS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS USING PROVIDED DATA.
   C. APPLY TEST STAMP IN NON-LEGEND AREA ON REAR SIDE OF PCB; OK TO APPLY TO PANEL RAILS IF SPACE DOES NOT PERMIT.

7. FINAL FINISH:
   A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:
   A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
   B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCBS SHALL BE DELIVERED IN PANEL FORM, HOWEVER, THESE SPECIFICATIONS MAY BE CHANGED AS REQUIRED BY THE CONTRACT MANUFACTURER TO SUPPORT VOLUME ASSEMBLY REQUIREMENTS.

SEE BOM	SEE BOM
NEXT ASSY	USED ON
APPLICATION	

THE INFORMATION CONTAINED HEREIN IS CONFIDENTIAL AND PROPRIETARY TO CYPRESS SEMICONDUCTOR AND SHALL NOT BE REPRODUCED OR DISCLOSED IN WHOLE OR IN PART OR USED FOR ANY DESIGN, MANUFACTURE, OR OTHERWISE, EXCEPT WHEN SUCH USER POSSESSES AUTHORIZATION FROM CYPRESS

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN METRIC WITH INCHES IN BRACKETS
.XXX ±.064 [±.005] .XX ±.13 [±.01] ANGLES ±.5°

MATERIAL 2

FINISH 7

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN ANEHASTECH	03/06/19
ENGINEER GVCH	03/06/19
CHECKER GVCH	03/06/19
QA -	-
PROJ. ENG. -	-

CYPRESS EMBEDDED IN TOMORROW
198 CHAMPION COURT
SAN JOSE, CA 95134
(408) 943-2600

TITLE
PCB FABRICATION,
CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT

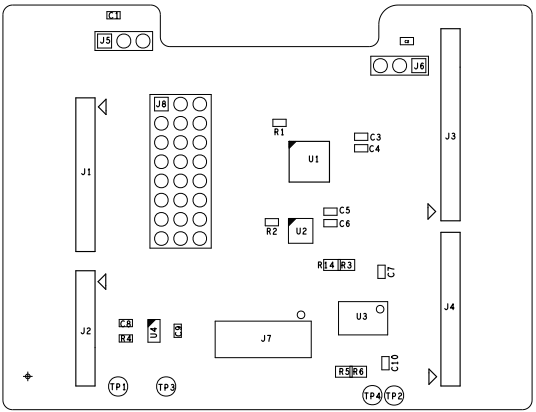
SIZE	CAGE CODE	CY P/N
D	-	610-60533-01

SCALE	SHEET	REV
1/1	1 OF 1	02

COMPUTER GENERATED DRAWING
DO NOT CHANGE MANUALLY

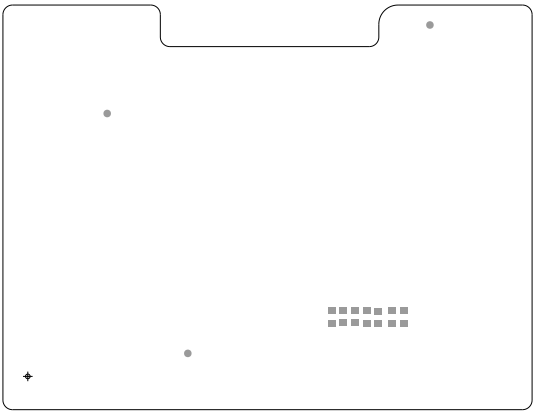
ALLEGRO FILE: 600-60533-01.BRD

ART FILM - Detail1



CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: ASSEMBLY TOP		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

ART FILM - SPB



CYPRESS EMBEDDED IN TOMORROW SAN JOSE, CA 95134 (408) 943-2600	PROJECT: CY15FRAMKIT-002 SERIAL F-RAM DEVELOPMENT KIT		
	DRAWN BY: ANEHASTECH		
	LAYER: SOLDERPASTE BOTTOM		
	DWG NO: 610-60533-01	REV: 02	DATE: 03/06/19

ART FILM - SPB